

Figure 1a

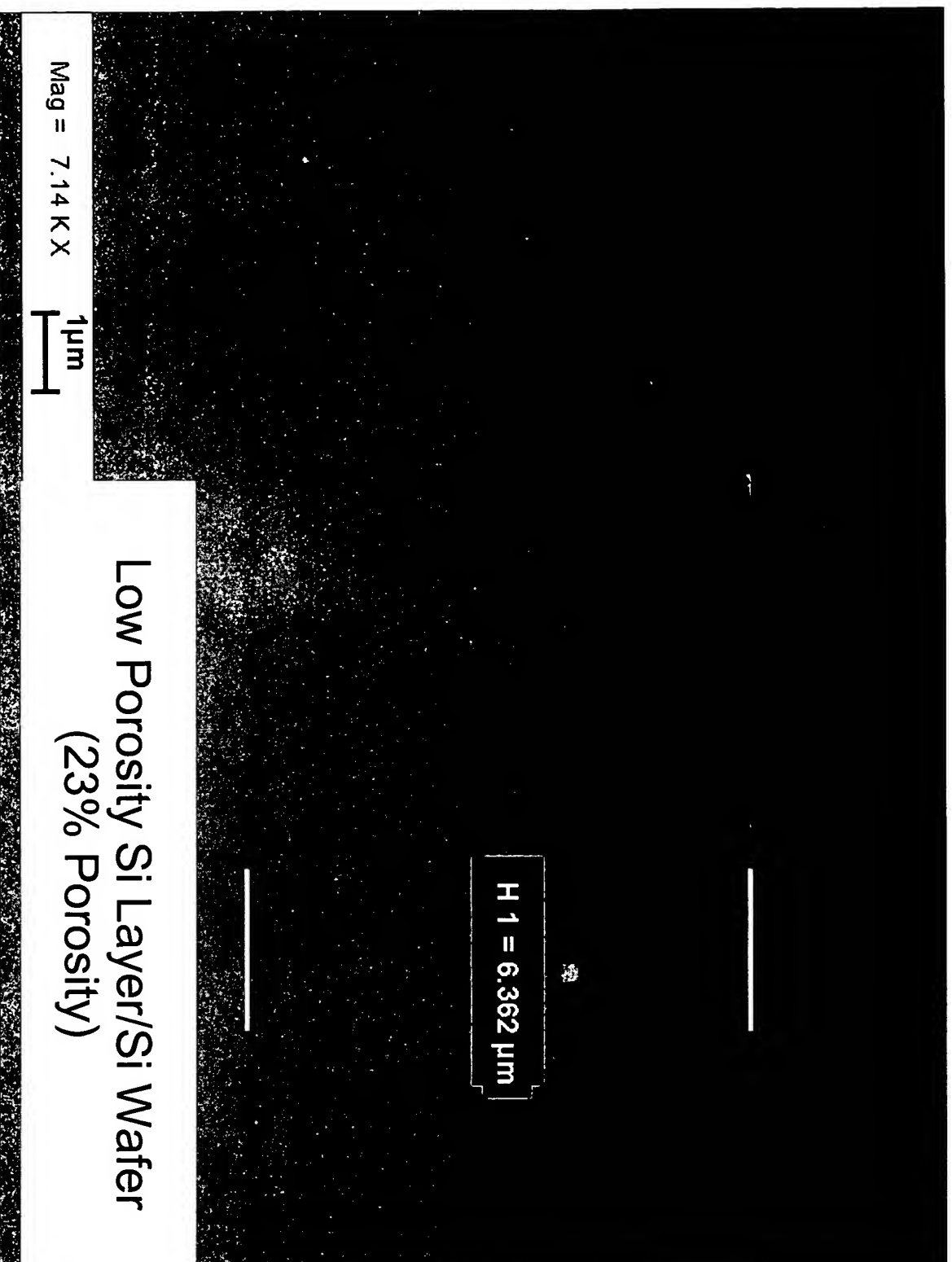


Figure 1b

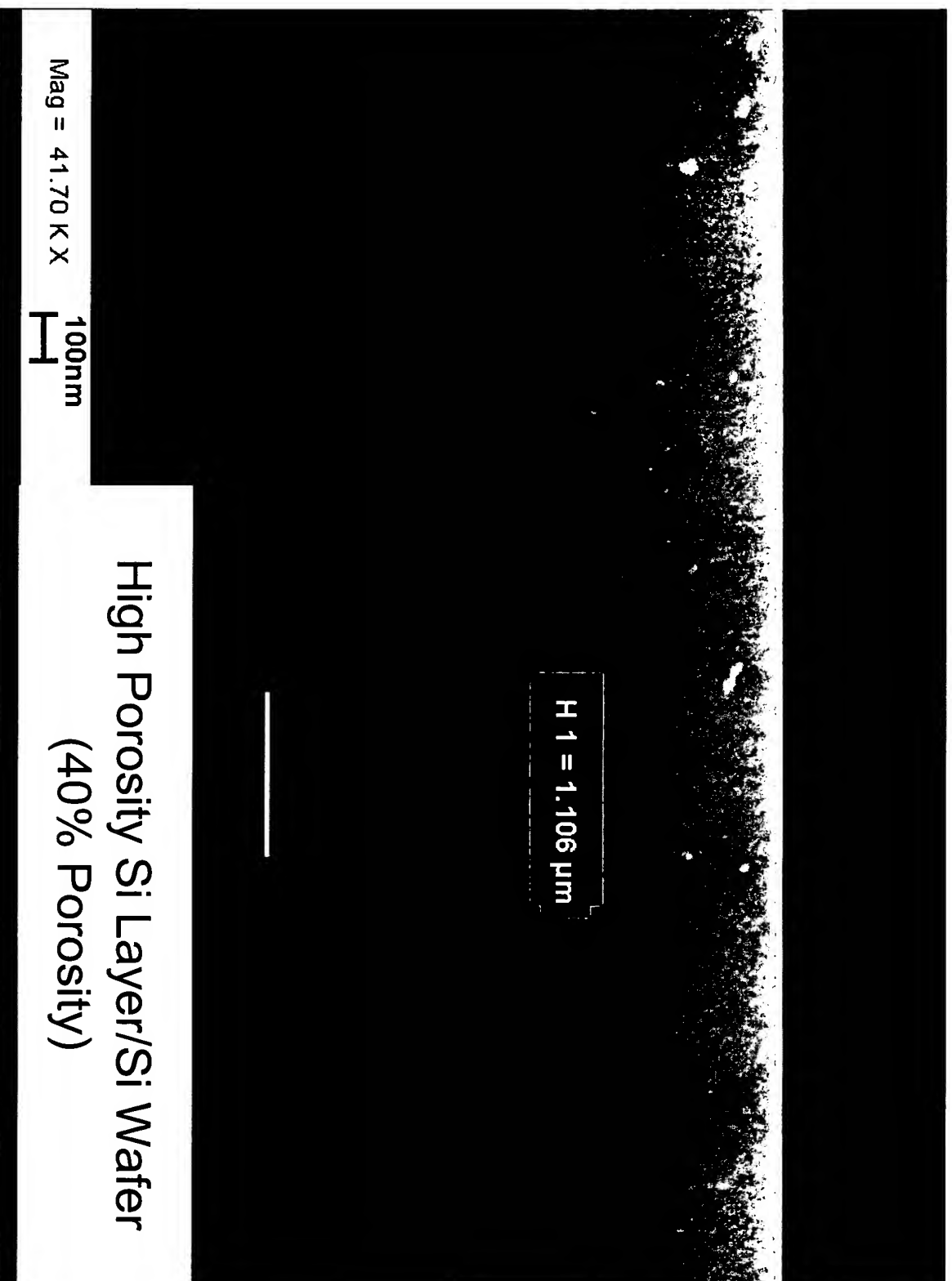


Figure 1c

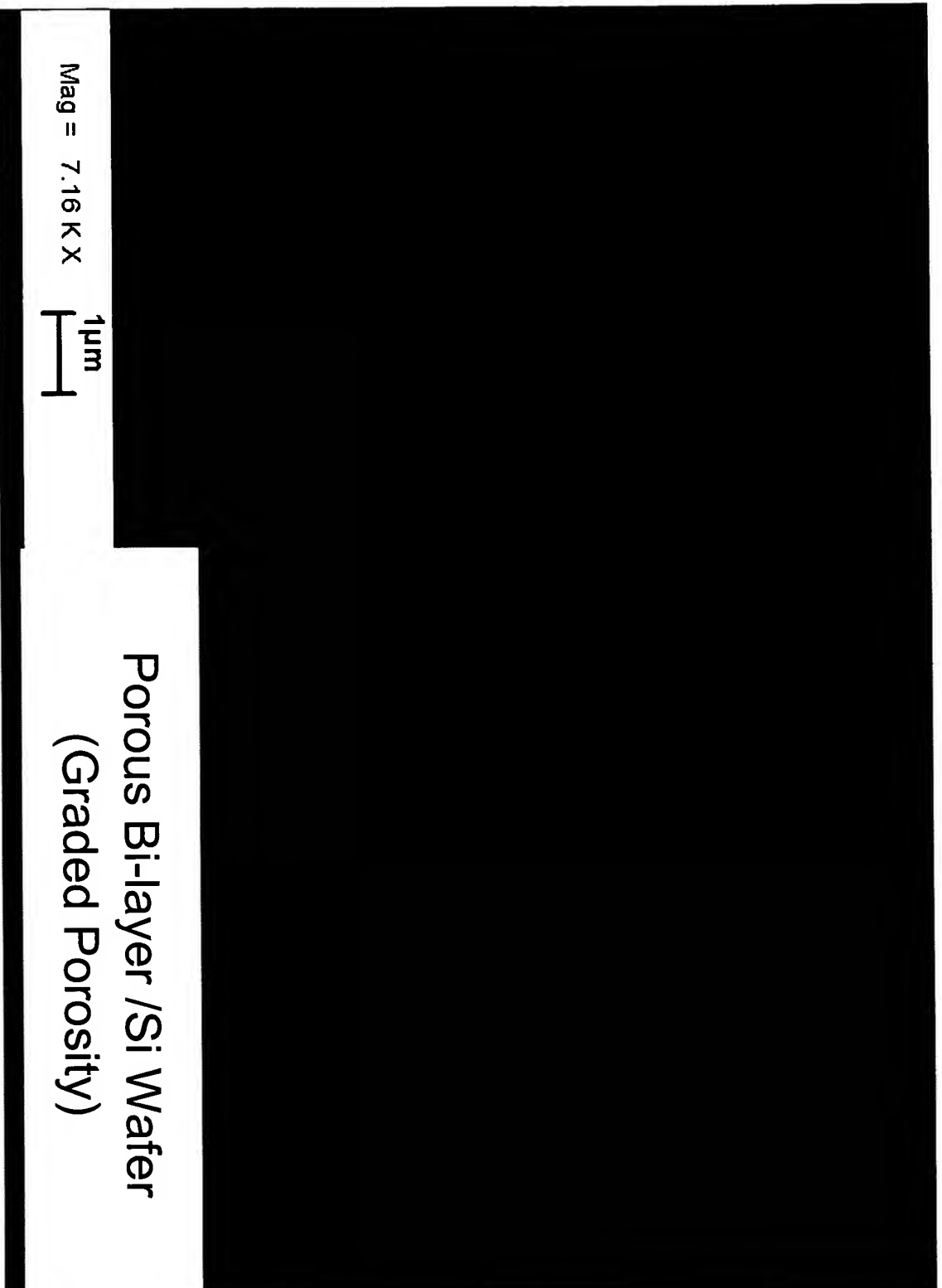
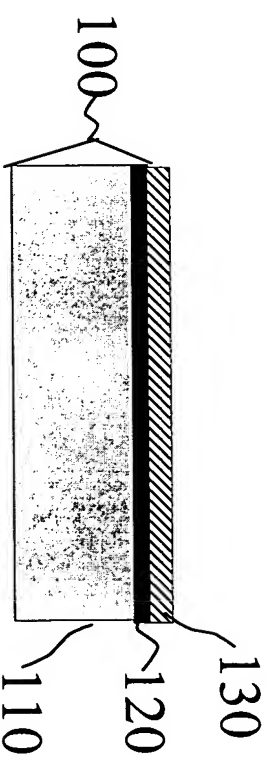


Figure 2



**substrate based on use of the porous-Si layer
and subsequent regrowth of epi-Si layer to create SOI wafers**

Figure 3

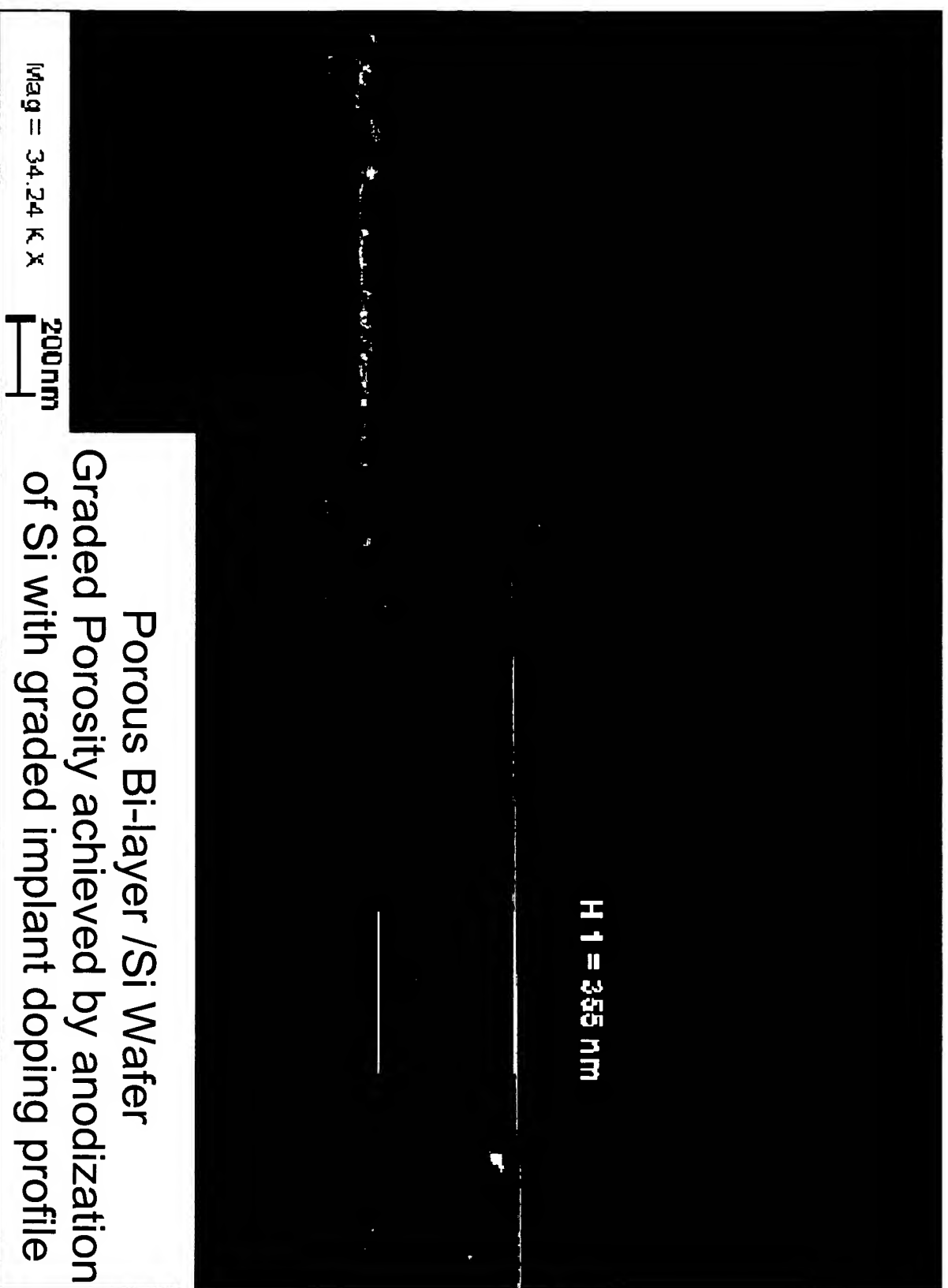


Figure 4

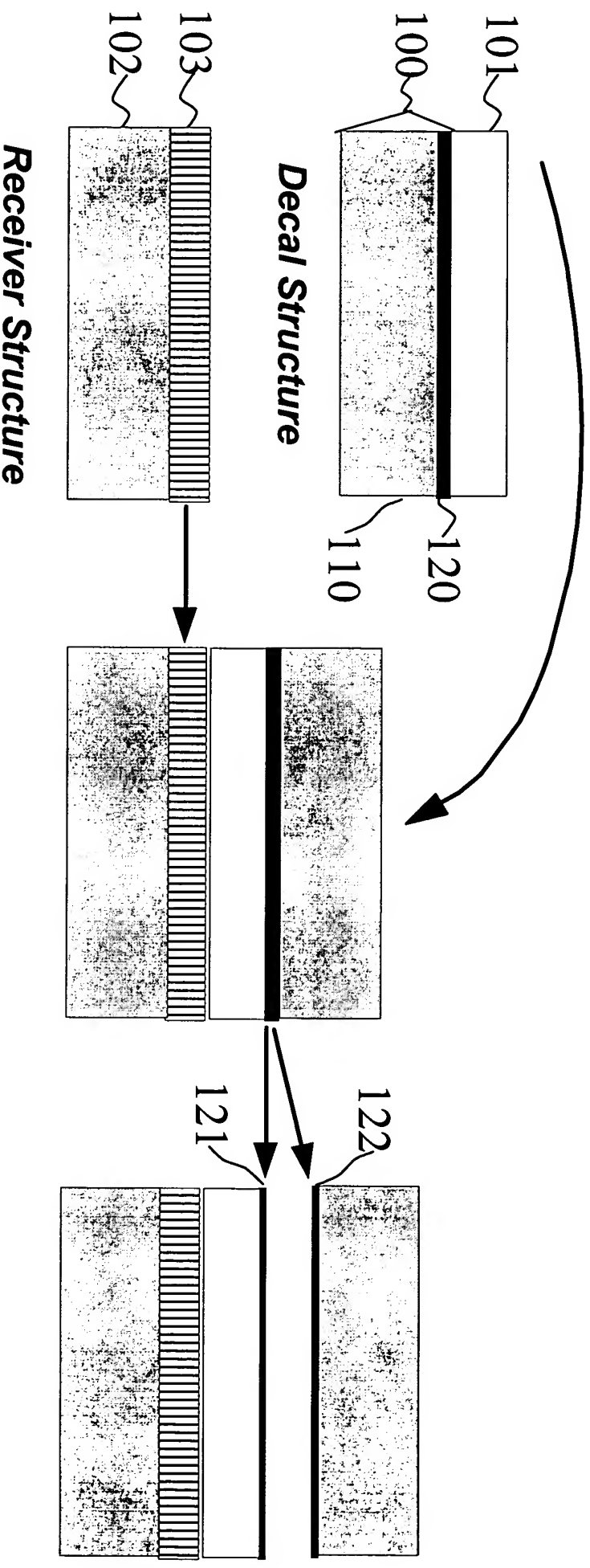
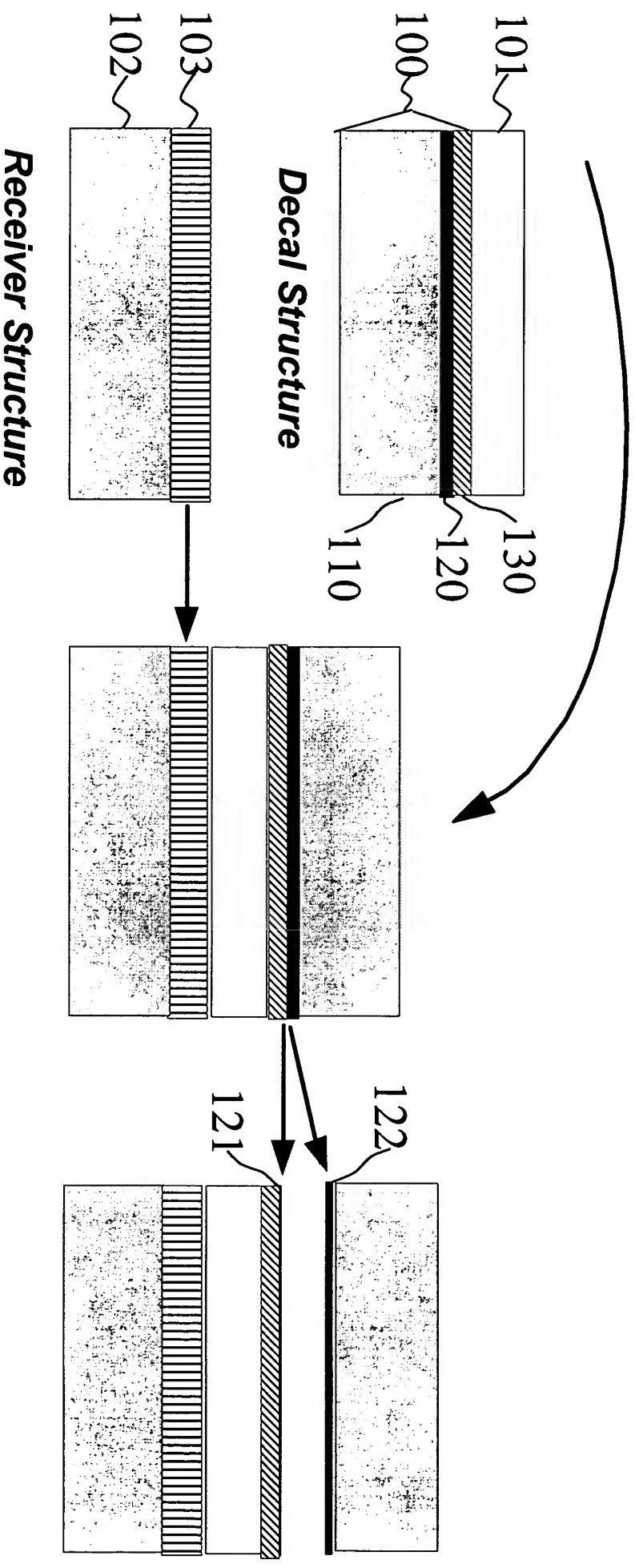


Figure 5



**#1 Step: Build of Decal
& Receiver Structures**

**#2 Step: Mating of Decal
& Receiver Structures**

**#3 Step: Release of Carrier
Substrate via Peeling**